ABSTRACT OF THE INVENTION

A signal processing circuit used in a hard disk controller is able to quickly match its clock signal with preamble data read from a hard disk. The signal processing circuit includes a decision feedback equalizer (DFE) that equalizes a digital read signal in accordance with a clock signal. A timing recovery PLL generates the clock signal having a phase which is coincident with a phase of the digital read signal. The DFE includes a first filter for filtering the digital signal, a decision circuit for adding a feedback signal to the filtered digital signal and generating a decision signal based on the value of the addition. A shift register is connected to the decision circuit and samples the decision signal in accordance with the clock signal, and stores the sampled signal as sampling data. A feedback filter filters the sampled data and feeds it back to the decision circuit. A loop control circuit monitors the filtered digital signal and the feedback signal and controls the feedback loop based on the values of these signals.